IN THE CLAIMS:

The following is a complete listing of the claims in this application, reflects all changes currently being made to the claims, and replaces all earlier versions and all earlier listings of the claims:

1.-16. (Canceled)

17. (Currently Amended) A sensor chip formed on a single semiconductor chip, comprising:

an image pickup portion which includes a plurality of photoelectric conversion elements;

a scan circuit which reads out a signal from said image pickup portion;

a drive pulse generation circuit which generates a drive pulse for driving said scan circuit;

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a reference clock signal generation circuit which internally generates a first reference clock signal;

a terminal which externally inputs a second reference clock signal from outside said sensor chip; and

a switch connected to at least said reference clock signal generation circuit and said terminal, which effects switching ~~so that said drive pulse generation circuit generates the drive pulse for said scan circuit on the basis of one of the first reference clock signal and the second reference clock signal~~ between internally driving said image pickup portion and externally driving said image pickup portion.

18. (Previously Presented) A sensor chip according to claim 17, wherein said drive pulse generation circuit generates a first pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a first mode, and a second pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a second mode, and wherein said sensor chip further comprises a first control circuit which effects control so that said drive pulse generation circuit generates the first pulse, and a terminal which inputs a control signal from outside said semiconductor chip for controlling said drive pulse generation circuit so as to generate the second pulse.

19. (Previously Presented) A sensor chip according to claim 18, wherein the first mode is a mode for reading out the signal from said image pickup portion at a resolution lower than that of the second mode.

B1 Cont.

20. (Currently Amended) A drive pulse generation chip formed on a single semiconductor chip, comprising:

a drive pulse generation circuit which generates a drive pulse;

a reference clock signal generation circuit which internally generates a first reference clock signal;

a terminal which externally inputs a second reference clock signal from the external of said drive pulse generation chip; and

a switch connected to at least said reference clock signal generation circuit and said terminal, which effects switching ~~so that said drive pulse generation circuit generates the drive pulse on the basis of one of the first reference clock signal and the second~~

~~reference clock signal~~ between internally driving said drive pulse generation circuit and externally driving said drive pulse generation circuit.

21. (Previously Presented) A drive pulse generation chip according to claim 20, wherein said drive pulse generation circuit generates a first pulse for a first drive mode and a second pulse for a second drive mode, and

wherein said drive pulse generation chip further comprises a first control circuit which effects control so that said drive pulse generation circuit generates the first pulse, and a terminal which inputs a control signal from outside said drive pulse generation chip for controlling said drive pulse generation circuit so as to generate the second pulse.

B1 Cont.

22. (Currently Amended) An image pickup apparatus comprising:

a sensor chip formed on a single semiconductor substrate,

said sensor chip comprising:

an image pickup portion which includes a plurality of photoelectric conversion elements;

a scan circuit which reads out a signal from said image pickup portion;

a drive pulse generation circuit which generates a drive pulse for driving said scan circuit, said drive pulse generation circuit generating a first pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a first mode, and a second pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a second mode;

a reference clock signal generation circuit which internally generates a first reference clock signal;

a terminal which externally inputs a second reference clock signal from outside said semiconductor substrate;

a switch connected to at least said reference clock signal generating circuit and said terminal, which effects switching ~~so that said drive pulse generation circuit generates the drive pulse of said scan circuit on the basis of one of the first reference clock signal and the second reference clock signal~~ between internally driving said image pickup portion and externally driving said image pickup portion; and

B1 Cont'd.

a first control circuit which effects control so that said drive pulse generation circuit generates the first pulse,

wherein said image pickup apparatus further ~~comprising~~ comprises a second control circuit which is provided externally to said semiconductor substrate and effects control so that said drive pulse generation circuit generates the second pulse.